WHAT IS CLAIMED IS:

1. A memory controller for coupling to a memory and for coupling to receive an address of a memory transaction, the memory controller comprising:

one or more registers programmable with an indication of which portion of said address is used to select a storage location in said memory for access in response to said memory transaction; and

a circuit coupled to said one or more registers and coupled to receive said address, wherein said circuit is configured to extract said portion of said address for transmission to said memory responsive to said indication in said one or more registers.

2. The memory controller as recited in claim 1 wherein said memory is arranged into rows and columns of storage locations, and wherein said portion of said address includes a first portion of said address used to select one of said rows and a second portion of said address used to select one of said columns, and wherein said indication identifies said first portion and said second portion.

3. The memory controller as recited in claim 2 wherein said memory controller is configured to transmit said first portion to said memory separate from said second portion.

4. The memory controller as recited in claim 3 wherein said memory controller is configured to transmit said first portion to said memory at a different time than said second portion.

5. The memory controller as recited in claim 2 wherein said indication includes a first bit

mask, wherein each bit of said first bit mask corresponds to at least one bit of said address, and wherein said circuit is configured to selectively include a first bit of said address in said first portion responsive to a corresponding bit of said first bit mask.

6. The memory controller as recited in claim 5 wherein said indication includes a second bit mask, wherein each bit of said second bit mask corresponds to at least one bit of said address, and wherein said circuit is configured to selectively include a second bit of said address in said second portion responsive to a corresponding bit of said second bit mask.

7. The memory controller as recited in claim 2 wherein said indication includes a first bit mask, wherein each bit of said first bit mask corresponds to a bit of said address, and wherein said circuit is configured to selectively include a first bit of said address in said first portion responsive to a corresponding bit of said first bit mask.

8. The memory controller as recited in claim 7 wherein said indication includes a second bit mask, wherein each bit of said second bit mask corresponds to a bit of said address, and wherein said circuit is configured to selectively include a second bit of said address in said second portion responsive to a corresponding bit of said second bit mask.

9. The memory controller as recited in claim 2 wherein said memory is further arranged into banks, and wherein said portion of said address includes a third portion used to select one of said banks, and wherein said indication identifies said third portion.

10. The memory controller as recited in claim 9 wherein said memory controller is configured to transmit said third portion separate from said first portion and said second portion.

11. The memory controller as recited in claim 9 wherein said indication comprises a third bit mask, wherein each bit of said third bit mask corresponds to at least one bit of said

address, and wherein said circuit is configured to selectively include a third bit of said address in said third portion responsive to a corresponding bit of said third bit mask.

12. The memory controller as recited in claim 9 wherein said indication comprises a third bit mask, wherein each bit of said third bit mask corresponds to a bit of said address, and wherein said circuit is configured to selectively include a third bit of said address in said third portion responsive to a corresponding bit of said third bit mask.

13. The memory controller as recited in claim 1 wherein said memory is arranged into two or more memory sections, and wherein said memory controller is configured to provide a different select signal to each of said memory sections to select said memory sections to respond to said memory transaction, and wherein said one or more registers are further programmable with an interleave mode for said memory sections.

14. The memory controller as recited in claim 13 wherein said interleave mode is no interleave.

15. The memory controller as recited in claim 13 wherein said interleave mode is interleave of a subset of said memory sections and no interleave of remaining ones of said memory sections.

16. The memory controller as recited in claim 13 wherein said interleave mode is interleave of said memory sections.

17. The memory controller as recited in claim 13 wherein said portion of said address further includes a fourth portion of said address which is used to select one of said interleaved memory sections, and wherein said indication identifies said fourth portion.

18. The memory controller as recited in claim 17 wherein said indication comprises a

fourth bit mask, wherein each bit of said fourth bit mask corresponds to at least one bit of said address, and wherein said circuit is configured to selectively include a fourth bit of said address in said fourth portion responsive to a corresponding bit of said fourth bit mask.

19. The memory controller as recited in claim 17 wherein said indication comprises a fourth bit mask, wherein each bit of said fourth bit mask corresponds to a bit of said address, and wherein said circuit is configured to selectively include a fourth bit of said address in said fourth portion responsive to a corresponding bit of said fourth bit mask.

20. The memory controller as recited in claim 13 wherein said one or more registers are further programmable with a different page mode policy for each of said memory sections.

21. The memory controller as recited in claim 1 wherein said memory is arranged in two or more independent memory sections, and wherein said memory controller is configured to provide a separate channel to each of said memory sections, and wherein said one or more registers are further programmable with a channel interleave indication indicating whether or not one or more of said channels are interleaved.

22. The memory controller as recited in claim 21 wherein said channel interleave indication further indicates a fifth portion of said address used to select one of said channels if one or more of said channels are interleaved.

23. A system comprising:

a memory; and

a memory controller coupled to said memory and to receive an address of a

memory transaction, the memory controller programmable with an indication of which portion of said address is used to select a storage location in said memory for access in response to said memory transaction, and wherein said memory controller is configured to extract said portion of said address for transmission to said memory responsive to said indication.

24. The system as recited in claim 23 wherein said memory is arranged into rows and columns of storage locations, and wherein said portion of said address includes a first portion of said address used to select one of said rows and a second portion of said address used to select one of said columns, and wherein said indication identifies said first portion and said second portion.

25. The system as recited in claim 24 wherein said memory controller is configured to transmit said first portion to said memory separate from said second portion.

26. The system as recited in claim 25 wherein said memory controller is configured to transmit said first portion to said memory at a different time than said second portion.

27. The system as recited in claim 24 wherein said indication includes a first bit mask, wherein each bit of said first bit mask corresponds to at least one bit of said address, and wherein said memory controller is configured to selectively include a first bit of said address in said first portion responsive to a corresponding bit of said first bit mask.

28. The system as recited in claim 27 wherein said indication includes a second bit mask, wherein each bit of said second bit mask corresponds to at least one bit of said address, and wherein said memory controller is configured to selectively include a second bit of said address in said second portion responsive to a corresponding bit of said second bit mask.

29. The system as recited in claim 24 wherein said indication includes a first bit mask, wherein each bit of said first bit mask corresponds to a bit of said address, and wherein said memory controller is configured to selectively include a first bit of said address in said first portion responsive to a corresponding bit of said first bit mask.

30. The system as recited in claim 29 wherein said indication includes a second bit mask, wherein each bit of said second bit mask corresponds to a bit of said address, and wherein said memory controller is configured to selectively include a second bit of said address in said second portion responsive to a corresponding bit of said second bit mask.

31. The system as recited in claim 24 wherein said memory is further arranged into banks, and wherein said portion of said address includes a third portion used to select one of said banks, and wherein said indication identifies said third portion.

32. The system as recited in claim 31 wherein said memory controller is configured to transmit said third portion to said memory separate from said first portion and said second portion.

33. The system as recited in claim 31 wherein said indication comprises a third bit mask, wherein each bit of said third bit mask corresponds to at least one bit of said address, and wherein said memory controller is configured to selectively include a third bit of said address in said third portion responsive to a corresponding bit of said third bit mask.

34. The system as recited in claim 31 wherein said indication comprises a third bit mask, wherein each bit of said third bit mask corresponds to a bit of said address, and wherein said memory controller is configured to selectively include a third bit of said address in said third portion responsive to a corresponding bit of said third bit mask.

35. The system as recited in claim 23 wherein said memory is arranged into two or more

memory sections, and wherein said memory controller is configured to provide a different select signal to each of said memory sections to select said memory section to respond to said memory transaction, and wherein said memory controller is further programmable with an interleave mode for said memory sections.

36. The system as recited in claim 35 wherein said interleave mode is no interleave.

37. The system as recited in claim 35 wherein said interleave mode is interleave of a subset of said memory sections and no interleave of remaining ones of said memory section.

38. The system as recited in claim 35 wherein said interleave mode is interleave of said memory sections.

39. The system as recited in claim 35 wherein said portion of said address further includes a fourth portion of said address which is used to select one of said interleaved memory sections, and wherein said indication identifies said fourth portion.

40. The system as recited in claim 39 wherein said indication comprises a fourth bit mask, wherein each bit of said fourth bit mask corresponds to at least one bit of said address, and wherein said memory controller is configured to selectively include a fourth bit of said address in said fourth portion responsive to a corresponding bit of said fourth bit mask.

41. The system as recited in claim 39 wherein said indication comprises a fourth bit mask, wherein each bit of said fourth bit mask corresponds to a bit of said address, and wherein said memory controller is configured to selectively include a fourth bit of said address in said fourth portion responsive to a corresponding bit of said fourth bit mask.

42. The system as recited in claim 35 wherein said memory controller is further programmable with a different page mode policy for each of said memory sections.

43. The system as recited in claim 23 wherein said memory is arranged in two or more independent memory sections, and wherein said memory controller is configured to provide a separate channel to each of said memory sections, and wherein said memory controller is further programmable with a channel interleave indication indicating whether or not one or more of said channels are interleaved.

44. The system as recited in claim 43 wherein said channel interleave indication further indicates a fifth portion of said address used to select one of said channels if one or more of said channels are interleaved.

45. A method comprising:

programming a memory controller with an indication of which portion of an address of a memory transaction is used to select a storage location in a memory for access in response to said memory transaction;

receiving said address of said memory transaction in said memory controller; and

extracting said portion of said address responsive to said indication.

46. The method as recited in claim 45 wherein said memory is arranged into rows and columns of storage locations, and wherein said portion of said address includes a first portion of said address used to select one of said rows and a second portion of said address used to select one of said columns, and wherein said indication identifies said first portion and said second portion.

47. The method as recited in claim 46 further comprising transmitting said first portion to said memory separate from said second portion.

48. The method as recited in claim 46 wherein said indication includes a first bit mask, wherein each bit of said first bit mask corresponds to at least one bit of said address, the method further comprising selectively including a first bit of said address in said first portion responsive to a corresponding bit of said first bit mask.

49. The method as recited in claim 48 wherein said indication includes a second bit mask, wherein each bit of said second bit mask corresponds to at least one bit of said address, the method further comprising selectively including a second bit of said address in said second portion responsive to a corresponding bit of said second bit mask.

50. The method as recited in claim 46 wherein said indication includes a first bit mask, wherein each bit of said first bit mask corresponds to a bit of said address, the method further comprising selectively including a first bit of said address in said first portion responsive to a corresponding bit of said first bit mask.

51. The method as recited in claim 50 wherein said indication includes a second bit mask, wherein each bit of said second bit mask corresponds to a bit of said address, the method further comprising selectively including a second bit of said address in said second portion responsive to a corresponding bit of said second bit mask.

52. The method as recited in claim 46 wherein said memory is further arranged into banks, and wherein said portion of said address includes a third portion used to select one of said banks, and wherein said indication identifies said third portion, the method further comprising transmitting said third portion separate from said first portion and said second portion.

53. The method as recited in claim 52 wherein said indication comprises a third bit mask, wherein each bit of said third bit mask corresponds to at least one bit of said address, the method further comprising selectively including a third bit of said address in said third portion responsive to a corresponding bit of said third bit mask.

54. The method as recited in claim 52 wherein said indication comprises a third bit mask, wherein each bit of said third bit mask corresponds to a bit of said address, the method further comprising selectively including a third bit of said address in said third portion responsive to a corresponding bit of said third bit mask.

55. The method as recited in claim 45 wherein said memory is arranged into two or more memory sections, the method further comprising:

providing a different select signal to each of said memory sections to select said memory sections to respond to said memory transaction; and

programming said one or more registers are with an interleave mode for said memory sections.

56. The method as recited in claim 55 wherein said interleave mode is no interleave.

57. The method as recited in claim 55 wherein said interleave mode is interleave of a subset of said memory sections and no interleave of remaining ones of said memory section.

58. The method as recited in claim 55 wherein said interleave mode is interleave of said memory sections.

59. The method as recited in claim 55 wherein said portion of said address further

includes a fourth portion of said address which is used to select one of said interleaved memory sections, and wherein said indication identifies said fourth portion.

60. The method as recited in claim 59 wherein said indication comprises a fourth bit mask, wherein each bit of said fourth bit mask corresponds to at least one bit of said address, the method further comprising selectively including a fourth bit of said address in said fourth portion responsive to a corresponding bit of said fourth bit mask.

61. The method as recited in claim 59 wherein said indication comprises a fourth bit mask, wherein each bit of said fourth bit mask corresponds to a bit of said address, the method further comprising selectively including a fourth bit of said address in said fourth portion responsive to a corresponding bit of said fourth bit mask.

62. The method as recited in claim 55 wherein said one or more registers are further programmable with a different page mode policy for each of said memory sections.

63. The method as recited in claim 45 wherein said memory is arranged in two or more independent memory sections, the method further comprising:

providing a separate channel to each of said memory sections; and

programming one or more registers with a channel interleave indication indicating whether or not one or more of said channels are interleaved.

64. The method as recited in claim 63 wherein said channel interleave indication further indicates a fifth portion of said address used to select one of said channels if one or more of said channels are interleaved.